(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
04 January 2018 (04.01.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/004496 A1

(51) International Patent Classification:
H03K 17/22 (2006.01) *H03K 17/284* (2006.01)
H03K 17/30 (2006.01)

(21) International Application Number:
PCT/TR2017/050233

(22) International Filing Date:
01 June 2017 (01.06.2017)

(25) Filing Language: Turkish

(26) Publication Language: English

(30) Priority Data:
2016/09051 28 June 2016 (28.06.2016) TR

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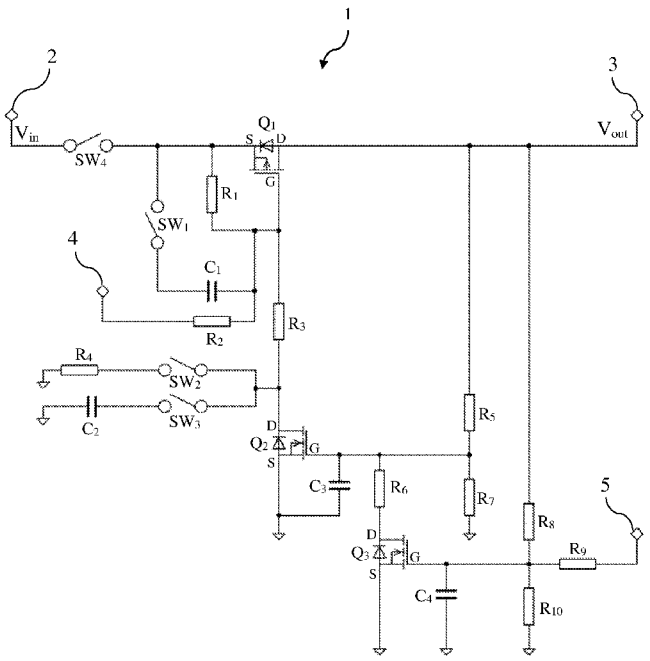
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,

WO 2018/004496 A1

(54) Title: A CONFIGURABLE LATCH CIRCUIT WITH LOW LEAKAGE CURRENT AND INSTANT TRIGGER INPUT

FIGURE 1



(57) Abstract: The present invention relates to latch circuit (1) which is connected between a power source and a load, which can be adjusted such that it will be latched/not latched depending on the configuration of the switches during application of the power for the first time, which can be closed again in a certain time after it is latched, and which essentially comprises three MOSFETs, four switches, four capacitors, a power input, a power output, a trigger output, and a suspension input.

[Continued on next page]

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

A CONFIGURABLE LATCH CIRCUIT WITH LOW LEAKAGE CURRENT AND INSTANT TRIGGER INPUT

Field of the Invention

The present invention is a latch circuit design which is especially designed for products operating with batteries, which can be adjusted to various forms of operations, which has low leakage current and instant trigger input and which is comprised of discrete components. The circuit can be considered as an on/off switch which is connected in series between the power source and the load. When a short pulse is given through the trigger input, the circuit latches itself; it continues to transfer power to the load even if the trigger pulse is removed. After a while, it enters to open circuit state again. If desired, it can be enabled to stay in continuous closed circuit state via a control signal. The circuit can latch itself for one time as if a trigger signal has been driven when power is applied from the power supply for the first time depending on the chosen configuration. According to this choice, the current to be drawn by the circuit (the leakage current) from the power supply when it becomes open circuit can be adjusted, and it can be kept at μA or nA level. The designed circuit is suitable for systems which will wait for a trigger for a long time and which requires low stand-by current.

Background of the Invention

Latch topologies enable circuits to remain in open or closed state in accordance with an input signal, and circuits continue to maintain their last states even if the input signal is removed.

United States Patent Document no US5790961, an application known in the state of the art, discloses a circuit requiring a switch which comprises a microcontroller and latches itself mechanically. United States Patent Document no US6255875 B1, an application known in the state of the art, discloses a latch circuit which comprises four switches and for FET transistors.

In several embodiments known in the state of the art, on/off operations are performed in turn by using the same trigger input. The circuit which is applied for is opened from the trigger input, and if desired, it is closed back after a certain time or it can always be kept open with a control signal run from outside.

The Problems Solved with the Invention

The present invention particularly provides a latch circuit which enables to reduce the power consumptions of systems operating with battery in stand-by situations. For this purpose, depending on the selected configuration, a latch circuit with instant trigger input designed with discrete components is provided which can be adjusted such that it will be latched/not latched during the first time application of power, and which can be closed back in a certain time if desired after it is latched.

Detailed Description of the Invention

A latch circuit developed to fulfill the objectives of the present invention is illustrated in the accompanying figures, in which:
Figure 1 is the schematic of the latch circuit.
Figure 2 is the flow diagram showing the operating principle of the latch circuit.

The components shown in the figures are each given reference numbers as follows:

1. Latch circuit

R_1. First resistor

2. Input port
3. Output port
4. Trigger port
5. Suspension port
Q1. First MOSFET
Q2. Second MOSFET
Q_3. Third MOSFET
SW_1. First switch
SW_2. Second switch
SW_3. Third switch
SW_4. Fourth switch
V_{in}. Input voltage
V_{out}. Output voltage
D. Drain terminal
S. Source terminal
G. Gate terminal

R_2. Second resistor
R_3. Third resistor
R_4. Fourth resistor
R_5. Fifth resistor
R_6. Sixth resistor
R_7. Seventh resistor
R_8. Eighth resistor
R_9. Ninth resistor
R_{10}. Tenth resistor
C_1. First capacitor
C_2. Second capacitor
C_3. Third capacitor
C_4. Fourth capacitor

The inventive latch circuit (1), which is connected between a power source and the load, essentially comprises

- at least one input port (2) to which the power source to be switched is connected,
- at least one output port (3) to which the loads to switched on and off are connected,
- a first MOSFET (Q_1) which is connected between the input port (2) connected to the source terminal (S) and the output port (3) connected to the drain terminal (D),
- a fourth switch (SW_4) which is connected between the input port (2) and the source terminal (S) of the first MOSFET (Q_1),
- a first switch (SW_1) one terminal of which is between the fourth switch (SW_4) and the source terminal (S) of the first MOSFET (Q_1), and the other terminal

of which is connected to the gate terminal (G) of the first MOSFET (Q_1) through a first capacitor (C_1),

- a trigger port (4) which is connected to the gate terminal (G) of the first MOSFET (Q_1) through a second resistor (R_2), and to which the instantaneous trigger input is driven,
- a second MOSFET (Q_2) the drain terminal (D) of which is connected to the gate terminal (G) of the first MOSFET (Q_1) through a third resistor (R_3), and the source terminal (S) of which is connected to the ground,
- a second capacitor (C_2) which is connected between the drain terminal (D) of the second MOSFET (Q_2) and the ground through a third switch (SW_3),
- a second switch (SW_2) which is connected in series with a fourth resistor (R_4) on a branch which is parallel to a branch on which the third switch (SW_3) is present,
- a third capacitor (C_3) which is connected between the gate terminal (G) and the source terminal (S) of the second MOSFET (Q_2),
- a third MOSFET (Q_3) the drain terminal (D) of which is connected to the gate terminal (G) of the second MOSFET (Q_2) through a sixth resistor (R_6), and the source terminal (S) of which is connected to the ground,
- a fourth capacitor (C_4) which is connected between the gate terminal (G) of the third MOSFET (Q_3) and the ground,
- a suspension port (5) which is connected to the gate terminal (G) of the third MOSFET (Q_3) through a ninth resistor (R_9), and wherein the control signal is driven in order to prevent the latched circuit from entering to the closed state again.

The inventive latch circuit (1) the schematic of which is given in Figure 1 is designed with components comprised of MOSFET, transistors, resistors and capacitors that can easily be found in the market.

Ten resistors are used in the latch circuit (1). The arrangement of the said resistors is as follows: the first resistor (R_1) is connected between the source terminal (S)

and the gate terminal (G) of the first MOSFET (Q_1). The second resistor (R_2) is connected between the trigger port (4) and the gate terminal (G) of the first MOSFET (Q_1). The third resistor (R_3) is connected between the gate terminal (G) of the first MOSFET (Q_1) and the drain terminal (D) of the second MOSFET (Q_2). The fourth resistor (R_4) is connected between the second switch (SW_2) and the ground. One terminal of the fifth resistor (R_5) is connected between the output port (3) and the drain terminal (D) of the first MOSFET (Q_1), and its other end is connected to the gate terminal (G) of the second MOSFET (Q_2). The sixth resistor (R_6) is connected between the gate terminal (G) of the second MOSFET (Q_2) and the drain terminal (D) of the third MOSFET (Q_3). One terminal of the seventh resistor (R_7) is connected to the gate terminal (G) of the second MOSFET (Q_2) and its other terminal is connected to the ground. The eighth resistor (R_8) is connected between the output port (3) and the gate terminal (G) of the third MOSFET (Q_3). The ninth resistor (R_9) is connected between the suspension port (5) and the gate terminal (G) of the third MOSFET (Q_3). The tenth resistor (R_{10}) is connected between the gate terminal (G) of the third MOSFET (Q_3) and the ground.

The working principle of the said latch circuit (1) is given as flow diagram in Figure 2. The names of the states shown in Figure 2 are written as *italic* in the explanations below. Furthermore, in the flow diagram a switch being closed indicates that it is in conduction, that is it is in closed circuit state; and a switch being open indicates that it is not in conduction, that is it is in open circuit state.

The input port (2) shown in Figure 1 shows the power input of the circuit. The power source to be switched is connected to the said port. The output port (3) is the power output of the circuit. The loads to be switched on and off are connected to the said output. The designed switching circuit (1) can be considered as a serial switch connected to the positive line. Within this context, the input of the switch is the input port (2), and its output is the output port (3). The trigger port (4) is an active low port from which the circuit receives instantaneous trigger. The

suspension port (5) is an active low control port which controls the operation of the timer part which causes the circuit to enter to open circuit state after a certain time from the closed circuit state.

Other switches (the first switch (SW_1), the second switch (SW_2) and the third switch (SW_3)) except from the fourth switch (SW_4) located in the latch circuit (1) are put in order to show that the latch circuit (1) can be adjusted in different configurations. After the operation configuration is determined, there is no situation which requires the use of the said switches. By considering the positions of the switches in the desired configuration, the circuit can be fixed and the switches can be removed. The fourth switch (SW_4) is included in order to emulate application of the input power. When the fourth switch (SW_4) is open, the circuit will enter to the *Closed* state whatever the state shown in Figure 2 is.

The latch circuit (1) can be adjusted such that it will be *Closed Circuit or Open Circuit* independent from the trigger input with the help of the first switch (SW_1), the second switch (SW_2) and the third switch (SW_3) after the fourth switch (SW_4) is closed. This selection is essentially performed with adjusting the C_{GSQ1}/C_{DSQ2} ratio. The said capacitances show the capacitances between the gate terminal (G) – source terminal (S) of the first MOSFET (Q_1) and the drain terminal (D) – source terminal (S) of the second MOSFET (Q_2), respectively. The said capacitances are essentially comprised of parasitic capacitances of the MOSFETs when the first switch (SW_1) and the third switch (SW_3) are open. When the first switch (SW_1) is closed, C_{GSQ1} is comprised of the first capacitor (C_1) and the parasitic capacitance of the gate terminal (G) – source terminal (S) of the first MOSFET (Q_1). Similarly, when the third switch (SW_3) is closed, C_{DSQ2} is comprised of the second capacitor (C_2) and the drain terminal (D) – source terminal (S) parasitic capacitance of the second MOSFET (Q_2). Although the parasitic capacitances of the MOSFETs are not under the control of the user, capacitors such as the first capacitor (C_1) and the second capacitor (C_2) can be connected and disconnected so that the C_{GSQ1}/C_{DSQ2} ratio can be changed.

When the fourth switch (SW_4) is closed, if the condition that the voltage between the source terminal (S) – gate terminal (G) of the first MOSFET (Q_1) is higher than the threshold voltage of the first MOSFET (Q_1) ($V_{SGQ1} > |V_{thQ1}|$) is provided for a sufficient time period, the output voltage (V_{out}) will start increasing to the input voltage (V_{in}) value. At the same time the voltage on third capacitor (C_3) will increase in a level the value of which is determined by the seventh resistor (R_7), the fifth resistor (R_5) and the output voltage (V_{out}) through the fifth resistor (R_5). If the conduction time of the first MOSFET (Q_1) is long enough, the condition that the voltage between the gate terminal (G) – source terminal (S) of the second MOSFET (Q_2) is higher than the threshold voltage of the second MOSFET (Q_2) ($V_{GSQ2} > V_{thQ2}$) can be obtained. In this case, the second MOSFET (Q_2) will start to conduct. When the ratio of the resistance value of first resistor (R_1) to the resistance value of third resistor (R_3) (R_1/R_3) is selected high enough, the voltage dropped on the first resistor (R_1) due to the current that will pass through the second MOSFET (Q_2) will keep the first MOSFET (Q_1) in conduction. Under these conditions as long as the first MOSFET (Q_1) is in conduction, the second MOSFET (Q_2) will also be in conduction; and thus the output voltage (V_{out}) will almost be equal to the input voltage (V_{in}) ($V_{out} \approx V_{in}$) since both transistors will keep themselves in conduction. At this point, the latch circuit (1) latches itself. In the meantime, the fourth capacitor (C_4) continues to charge just as the third capacitor (C_3). For proper operation, upon voltage increase on the fourth capacitor (C_4), the condition that the voltage between the gate terminal (G) – source terminal (S) of the third MOSFET (Q_3) is higher than the threshold voltage of the third MOSFET (Q_3) ($V_{GSQ3} > V_{thQ3}$) should be satisfied in much later time that the condition of $V_{GSQ2} > V_{thQ2}$ upon the voltage increase on the third capacitor (C_3). Therefore, the values of the components should be selected in this way. While the second MOSFET (Q_2) being in conduction latches the circuit, the third MOSFET (Q_3) will force the second MOSFET (Q_2) to cut-off conduction when it starts conducting. When the second MOSFET (Q_2) stops conduction, the first MOSFET (Q_1) will also stop the conduction and output voltage (V_{out}) will approximately be

0V ($V_{out} \approx 0V$). In order that the circuit will close itself back after a certain time; the values of the fifth resistor (R_5) and the seventh resistor (R_7) should be selected such that the value of the parallel equivalent resistance they form will be much higher ($R_6 << R_5 // R_7$) than the value of the sixth resistor (R_6). After a certain time the latch circuit (1) latches itself, it can close itself. However, the said closing can be stopped if desired. The closing feature is controlled via the suspension port (5). When the condition that the parallel equivalent resistance value formed by the eighth resistor (R_8) and the tenth resistor (R_{10}) is much higher ($R_9 << R_8 // R_{10}$) than the value of the ninth resistor (R_9) is met, if the suspension port (5) is kept at low level from the outside (if low level voltage is applied), the fourth capacitor (C_4) will not be charged and the third MOSFET (Q_3) cannot conduct in this time period. This enables the circuit to remain latched. If it is considered that there is an intelligent component on the part which is powered by the circuit, this component can keep the suspension port (5) in low level as long as power is required. When the power is desired to be cut off, the suspension port (5) is left at floating level. After this point, when the fourth capacitor (C_4) is charged sufficiently, the third MOSFET (Q_3) will start conduction and inhibit the latch structure. At this point, the circuit will remain in *Open Circuit* state shown in Figure 2.

The trigger port (4) of the circuit is used for entering to *Closed Circuit* state from the *Open Circuit* state. When signal in a sufficient length is applied from there, the first MOSFET (Q_1) will start conduction, and the circuit will start operating as described above. The second resistor (R_2) is used to limit the current that will flow into the trigger source (trigger port (4)) at a safe value. The trigger signal should remain in low level long enough to allow the formation of latch structure. Since the circuit can latch itself after this point, the trigger signal can be removed. Applying a high level trigger signal can cause the circuit to close before time out (before the third MOSFET (Q_3) starts conduction). If this is desired, the voltage level of the closing signal to be applied from the trigger input should be selected considering the input voltage (V_{in}), the first resistor (R_1), the second resistor (R_2)

and the third resistor (R_3). Even if the circuit topology will allow this usage, in the design objective of the invention the trigger input is only for enabling transition from *Open Circuit* state to *Closed Circuit* state.

Consider that the circuit is configured to latch itself when power is applied (that is in case the fourth switch (SW_4) is closed). In order to realize this situation, as stated before, C_{GSQ1}/C_{DSQ2} ratio should be adjusted properly. When this ratio is much smaller than one ($<<1$), it can be thought that the circuit will steadily show this characteristic. The value of parasitic capacitances of other circuit elements and MOSFETs has great importance in determining the suitable ratio. In order to provide this condition, the third switch (SW_3) is closed and C_{DSQ2} is increased (by connecting the second capacitor (C_2)) and the C_{GSQ1} capacitance is kept at a lower value by leaving the first switch (SW_1) open. Let's consider that the circuit can latch itself when power is given in this way. Think that the circuit will bring itself to *Open Circuit* state with time out feature after a certain time after power is applied. While waiting in this way, the circuit will enter to *Closed* state when the input power of the circuit is removed. Then, when the power is applied immediately, the circuit may not latch itself even though the *First Power Option* is *Closed Circuit*. The reason for this is that the second capacitor (C_2) is charged nearly to output voltage (V_{in}) level after the second MOSFET (Q_2) stops conduction when the circuit enters to *Open Circuit* state. However, V_{GSQ1} and V_{DSQ2} voltages should nearly be 0V so that the circuit can latch itself when the power is applied. The second capacitor (C_2) can only be discharged by its internal leakage current and the through the second MOSFET (Q_2). This discharge rate may not be suitable for the purpose for which the circuit will be used. If the discharge is not realized, the circuit cannot latch itself when the power is applied again.

For this, a discharge resistor which is a fourth resistor (R_4) that can be selected with the second switch (SW_2) is added. This resistor discharges the second capacitor (C_2) after entering to *Closed* state. The discharge rate will increase as

the resistance value of the fourth resistor (R_4) decreases and the recovery time required for the circuit to enter to the *Closed Circuit* state by latching itself when power is applied after entering to the *Closed* state decreases. However, the value of the said fourth resistor (R_4) increases the current (leakage current) drawn by the circuit from the input in *Open Circuit* state. A current will flow through the first resistor (R_1), third resistor (R_3) and fourth resistor (R_4) in the *Open Circuit* state. The resistance values should be selected considering a balance between the recovery time of the circuit and the leakage current. If the circuit is configured such that it will be in the *Open Circuit* state when power is applied, there will be no use of using the said resistance as well as there will be a disadvantage of increasing the leakage current.

If it is wanted to configure the circuit such that it will not latch itself when power is applied (that is when the fourth switch (SW_4) is closed), $C_{GSQ1}/C_{DSQ2} >> 1$ condition should be provided for stable operation. In order to provide this, the first switch (SW_1) is closed, and C_{GSQ1} capacitance is increased by means of the first capacitor (C_1). At the same time, the third switch (SW_3) is kept open, and thus the C_{DSQ2} capacitance is kept at a lower value. As it is stated before, in this case it is not required to connect the fourth resistor (R_4), and leaving the second switch (SW_2) open will enable the leakage current to remain low.

The operation principle of the circuit expressed in Figure 2 can be explained as below by using the schematic in Figure 1:

The *Closed* state indicates that the fourth switch (SW_4) is open circuit, no power is applied to the circuit. When the fourth switch (SW_4) is closed, *Power is applied* event takes place. When the fourth switch (SW_4) is opened in any state, that is when the power of the circuit is cut off, the *Power off* event takes place and the circuit enters to *Closed* state. When the first switch (SW_1) is open and the third switch (SW_3) is closed, "*First Power Option*" will be *Closed Circuit* and the circuit will enter to *Closed Circuit* State as soon as the power is applied if the

component values are selected suitably. When the switches are adjusted in exact opposite way, "*First Power Option*" will be *Open circuit* and the circuit will enter to *Open Circuit* State as soon as the power is applied. *Closed Circuit* corresponds to the state where the first MOSFET (Q_1) is in conduction. In this case, the output voltage (V_{out}) at the output port (3) will nearly be equal to the input voltage (V_{in}) at the input port (2) ($V_{out} \approx V_{in}$). If the suspension port (5) will be kept at low level from outside in this state, the *Time Out* will be *Disabled* and the circuit will remain in *Closed Circuit* state. When the suspension port (5) is left at floating level, the *Time Out* will be *Enabled* and the circuit will enter to *Countdown* state. In this case, the first MOSFET (Q_1) will remain in conduction. However, in the meantime the fourth capacitor (C_4) will be charged. If the suspension port (5) is driven with low level signal before the voltage on this capacitor put the third MOSFET (Q_3) in conduction and reaches a level that will inhibit the latch structure, *Time Out Disabled* event takes places and it enters from *Countdown* state to *Closed Circuit* state. However, if the fourth capacitor (C_4) is charged enough so that the third MOSFET (Q_3) will start conduction in *Countdown* state, *Time is up* event takes place, and the circuit closes itself and enters to *Open Circuit* state. The first MOSFET (Q_1) will not be in conduction in *Open Circuit* state. In this case, it can be entered to *Closed Circuit* state with a low level trigger signal to be applied to the trigger port (4). If the circuit is configured such that the *First Power Option* will be *Closed Circuit*, it can be entered to *Closed Circuit* state again by alternatively realizing the *Power off* and then *Power is applied* events. In order to realize this transitions, as previously stated, it should be $V_{DSQ2} \approx 0V$. Otherwise, *First Power Option* will not operate properly. The fourth resistor (R_4) (discharge load) can be activated for discharge acceleration.

The circuit is built with the values and components given in Table 1, and the leakage currents are measured according to several circumstances.

Table 1. Exemplary values to be used for the components in the latch circuit

Reference	**Value / Type Number**
R_1	1 KΩ
R_2	100 Ω
R_3	100 Ω
R_4	10 MΩ
R_5	1 KΩ
R_6	20 Ω
R_7	10 KΩ
R_8	1 MΩ
R_9	100 Ω
R_{10}	1 MΩ
C_1	100 nF
C_2	100 + 22 = 122 nF
C_3	22 nF
C_4	22 µF
Q_1	SI7461DP
Q_2	2N7002
Q_3	2N7002

Table 2. Different configurations of circuit depending on the positions of the switches

Configuration	**SW_1**	**SW_2**	**SW_3**	**Explanation**
#1	Open	Closed	Closed	*First power option -> Closed circuit*, Discharge resistor active
#2	Open	Open	Closed	*First power option -> Closed circuit*, Discharge resistor deactivated
#3	Closed	Open	Open	*First power option -> Open circuit*, Discharge

				resistor deactivated

For the configurations given in Table 2, the leakage currents of the circuit built with materials given in Table 1 in *Open Circuit* state with measurements performed at ambient temperature of 25 °C are given in Table 3 for different operation voltages.

Table 3. The leakage currents of Latch Circuit (1) measured for different input voltages (V_{in})

V_{in} / Configuration	**#1**	**#2**	**#3**
5 VDC	0.4992 µA	1.1 nA	1.1 nA
9 VDC	0.9023 µA	1.5 nA	1.4 nA
12 VDC	1.2031 µA	2.1 nA	1.7 nA

CLAIMS

1. A latch circuit (1), which is connected between a power source and a load, which can be adjusted such that it will be latched/not latched depending on the configuration of the switches during application of the power for the first time, which can be closed again in a certain time after it is latched, essentially **characterized by**

- a first MOSFET (Q_1) which is connected between an input port (2) to which the power source to be switched to the source terminal (S) is connected and an output port (3) to which the loads to be switched on and off by being switched to the drain terminal (D),
- a fourth switch (SW_4) which is connected between the input port (2) and the source terminal (S) of the first MOSFET (Q_1),
- a first switch (SW_1) one terminal of which is between the fourth switch (SW_4) and the source terminal (S) of the first MOSFET (Q_1), and the other terminal of which is connected to the gate terminal (G) of the first MOSFET (Q_1) through a first capacitor (C_1),
- a trigger port (4) which is connected to the gate terminal (G) of the first MOSFET (Q_1) through a second resistor (R_2), and to which the instantaneous trigger input is given,
- a second MOSFET (Q_2) the drain terminal (D) of which is connected to the gate terminal (G) of the first MOSFET (Q_1) through a third resistor (R_3), and the source terminal (S) of which is connected to the ground,
- a second capacitor (C2) which is connected between the drain terminal (D) of the second MOSFET (Q_2) and the ground through a third switch (SW_3),
- a second switch (SW_2) which is connected in series to a fourth resistor (R_4) on a branch parallel to a branch on which the third switch (SW_3) is present,
- a third capacitor (C_3) which is connected between the gate terminal (G) and the source terminal (S) of the second MOSFET (Q_2),

- a third MOSFET (Q_3) the drain terminal (D) of which is connected to the gate terminal (G) of the second MOSFET (Q_2) through a sixth resistance (R_6), and the source terminal (S) of which is connected to the ground,
- a fourth capacitor (C_4) which is connected between the gate terminal (G) of the third MOSFET (Q_3) and the ground,
- a suspension port (5) which is connected to the gate terminal (G) of the third MOSFET (Q_3) through a ninth resistor (R_9), and wherein the control signal is given in order to prevent the latched circuit from entering to the closed state again.

2. A latch circuit (1) according to claim 1, **characterized by** first resistor (R_1) which is connected between the source terminal (S) and gate terminal (G) of the first MOSFET (Q1), and third resistor (R_3) which is connected between the gate terminal (G) of the first MOSFET (Q_1) and the drain terminal (D) of the second MOSFET (Q_2).

3. A latch circuit (1) according to claim 1, **characterized by** second resistor (R_2) which is connected between the trigger port (4) and the gate terminal (G) of the first MOSFET (Q_1), and which enables to limit the current to flow into the trigger port (4).

4. A latch circuit (1) according to claim 1, **characterized by** fourth resistor (R_4) which is connected between the second switch (SW_2) and the ground, and which enables the second capacitor (C_2) to discharge.

5. A latch circuit (1) according to claim 1, **characterized by** fifth resistor (R_5) one terminal of which is connected between the output port (3) and the drain terminal (D) of the first MOSFET (Q_1), and the other terminal of which is connected to the gate terminal (G) of the second MOSFET (Q_2), and a seventh resistor (R_7) one terminal of which is connected to the gate terminal (G) of the

second MOSFET (Q_2) and the other terminal of which is connected to the ground.

6. A latch circuit (1) according to claim 5, **characterized by** sixth resistor (R_6) which is connected between the gate terminal (G) of the second MOSFET (Q_2) and the drain terminal (D) of the third MOSFET (Q_3), and the value of which is smaller than the value of the parallel equivalent resistance formed by the fifth resistor (R_5) and the seventh resistor (R_7).

7. A latch circuit (1) according to claim 1, **characterized by** eighth resistor (R_8) which is connected between the output port (3) and the gate terminal (G) of the third MOSFET (Q_3), and a tenth resistor (R_{10}) which is connected between the gate terminal (G) of the third MOSFET (Q_3) and the ground.

8. A latch circuit (1) according to claim 7, **characterized by** ninth resistor (R_9) which is connected between the suspension port (5) and the gate terminal (G) of the third MOSFET (Q_3), and the value of which is smaller than the parallel equivalent resistance value formed by the eighth resistor (R_8) and the tenth resistor (R_{10}).

9. A latch circuit (1) according to claim 1, **characterized by** fourth switch (SW_4) which enables the input power to be applied/cut off.

10. A latch circuit (1) according to claim 9, **characterized by** first MOSFET (Q_1) which can start conduction when the fourth switch (SW_4) is closed.

11. A latch circuit (1) according to claim 10, **characterized by** second MOSFET (Q_2) which starts conduction after the first MOSFET (Q_1) starts conduction.

12. A latch circuit (1) according to claim 5, **characterized by** third capacitor (C_3) the value of which increases to a level determined by the fifth resistor (R_5),

seventh resistor (R_7) and output voltage (V_{out}) through the fifth resistor (R_5) upon the second MOSFET (Q_2) passing to the conduction.

13. A latch circuit (1) according to claim 1 or 2, **characterized by** first resistor (R_1) which keeps the first MOSFET (Q_1) with the voltage dropped thereon by means of the current passing through the second MOSFET (Q_2).

14. A latch circuit (1) according to claim 12, **characterized by** third MOSFET (Q_3) which stops the conduction of the second MOSFET (Q_2), when it is in conduction.

15. A latch circuit (1) according to claim 14, **characterized by** second MOSFET (Q_2) which stops the conduction of the first MOSFET (Q_1), when it stops its conduction.

16. A latch circuit (1) according to claim 1, **characterized by** suspension port (5) wherein low level voltage is applied enabling that the fourth capacitor (C_4) cannot be charged through the eighth resistor (R_8) in order to prevent the third MOSFET (Q_3) from starting conduction.

17. A latch circuit (1) according to claim 1 or 16, **characterized by** suspension port (5) which can be left at floating level in order to enable the third MOSFET (Q_3) to conduct and therefore inhibit the latch structure by charging the fourth capacitor (C_4).

18. A latch circuit (1) according to claim 15, **characterized by** trigger port (4) to which the signal to activate the first MOSFET (Q_1) for conduction for entering from *Open Circuit* state to *Closed Circuit* state.

19. A latch circuit (1) according to claim 15, **characterized by** trigger port (4) to which a high level trigger signal is given for closing the circuit before the third MOSFET (Q_3) starts conduction.

FIGURE 1

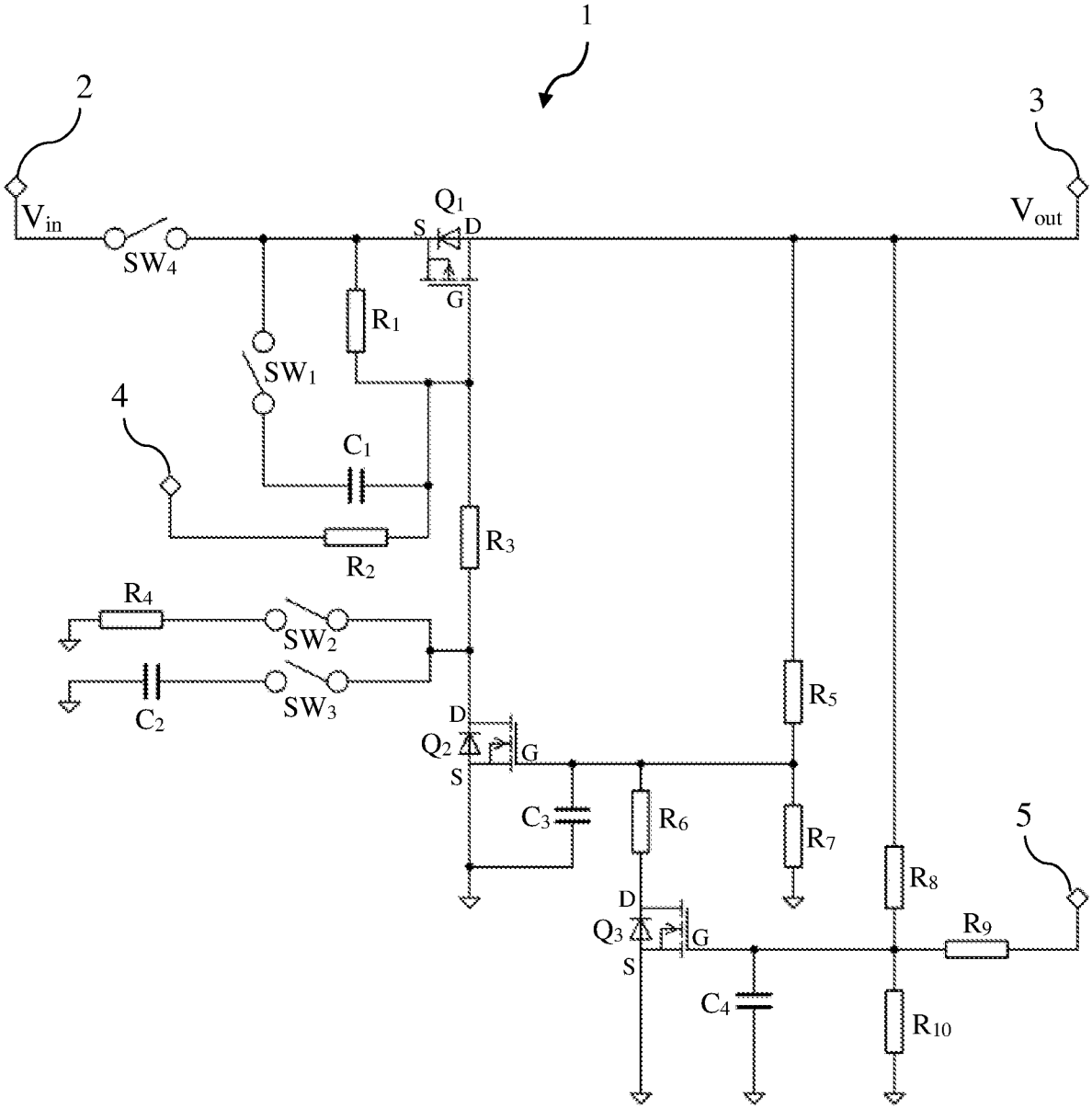
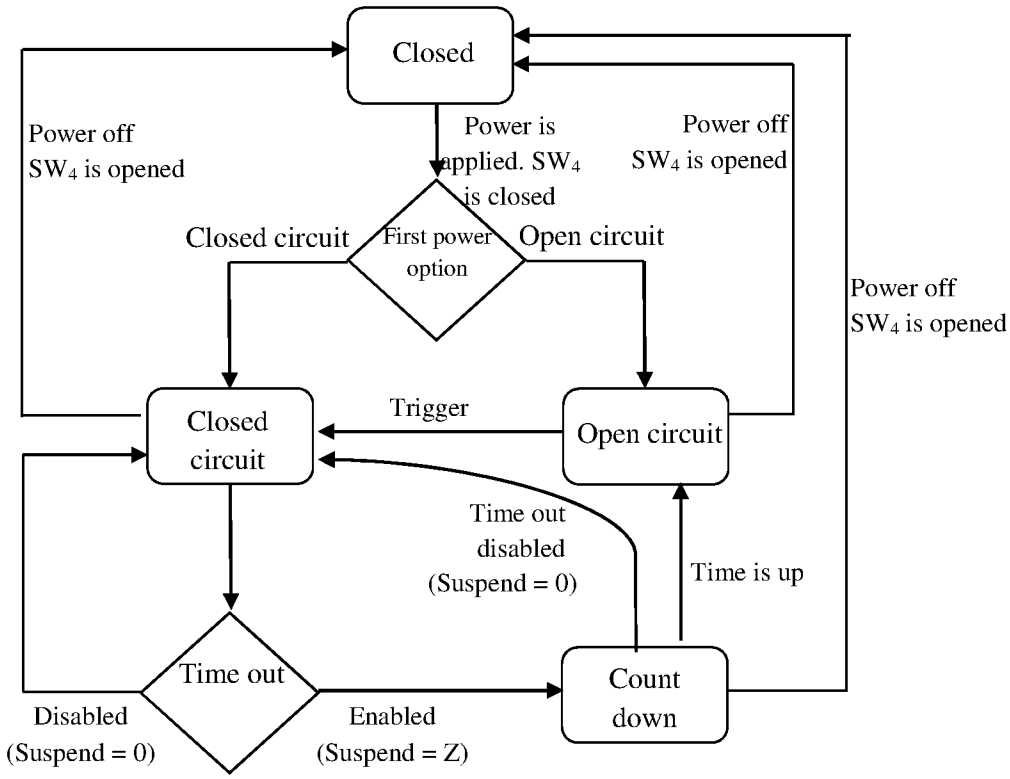

1
2
3
4
5
Vin
Vout
SW4
SW1
SW2
SW3
Q1
Q2
Q3
S
D
G
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
C1
C2
C3
C4

FIGURE 2


Closed
Power off
SW4 is opened
Power is
applied. SW4
is closed
Power off
SW4 is opened
Closed circuit
First power
option
Open circuit
Power off
SW4 is opened
Closed
circuit
Trigger
Open circuit
Time out
disabled
(Suspend = 0)
Time is up
Time out
Count
down
Disabled
(Suspend = 0)
Enabled
(Suspend = Z)

INTERNATIONAL SEARCH REPORT

International application No
PCT/TR2017/050233

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K17/22
ADD. H03K17/30 H03K17/284

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2007/040452 A1 (CHEN YUNG-FA [TW]) 22 February 2007 (2007-02-22) paragraph [0013] - paragraph [0019]; figures 1,2,3	1-3,5-19 4
A	US 2011/316609 A1 (CEGNAR ERIK J [US]) 29 December 2011 (2011-12-29) paragraph [0022] - paragraph [0029]; figure 1	1-19
Y A	US 2002/171464 A1 (STELLE RALEIGH B [US] ET AL) 21 November 2002 (2002-11-21) paragraph [0018] - paragraph [0019]; figure 1	4 1-3,5-19
A	US 2012/049832 A1 (SHINYAMA HIDEKI [JP]) 1 March 2012 (2012-03-01) abstract; figure 1	1-19

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 November 2017	07/12/2017

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/TR2017/050233

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